A Boundary Scan Test Vehicle for Direct Chip Attach Testing

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To facilitate the new faster, better and cheaper spacecraft designs, smaller more mass efficient avionics and instruments are using higher density electronic packaging technologies such as direct chip attach (DCA). For space flight applications, these technologies need to have demonstrated reliability and reasonably well defined fabrication and assembly processes before they will be accepted as baseline designs in new missions. As electronics shrink in size, not only can repair be more difficult, but "probing" circuitry can be very risky and it becomes increasingly more difficult to identify the specific source of a problem. To test and monitor these new technologies, the Direct Chip Attach Task, under NASA's Electronic Parts and Packaging Program (NEPP), chose the test methodology of boundary scan testing. The boundary scan methodology was developed for interconnect integrity and functional testing at hard to access electrical nodes. With boundary scan testing, active devices are used and failures can be identified to the specific device and lead. This technology permits the incorporation of "built in test" into almost any circuit and thus gives detailed test access to the highly integrated electronic assemblies. This presentation will describe boundary scan, discuss the development of the boundary scan test vehicle for DCA and current plans for testing of direct chip attach configurations.